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Kimton N. Eng, Esq.
DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101

EXAMINER	
CLEARY, THOMAS J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/994,516	Applicant(s) DOAN ET AL.	
	Examiner Thomas J. Cleary	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 November 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2, 3, 4, 5, 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 does not indicate whether the memory that the controller transfers data to the second bus from is the "memory coupled to the first bus to store data accessible by the CPU" or the "non-volatile memory for storing machine state information".

3. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 does not indicate whether the memory that the controller transfers data to the second bus from is the "memory coupled to the CPU to store data accessible by the CPU" or the "non-volatile memory for storing machine state information".

4. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. Claim 17 does not indicate whether the memory that the controller transfers data to the second bus from is the "memory [coupled to a CPU] via a first bus" or the "non-volatile memory for storing machine state information".

5. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 23 does not indicate whether the memory that the controller transfers data to the second bus from is the "memory [coupled to a CPU] via a first bus" or the "non-volatile memory for storing machine state information".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 5, 6, 8, 9, 12, 13, 15, 16, 17, 20, 22, 23, 26, 38, 42, 45, and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication Number 2003/0005223 to Coulson et al. ("Coulson").

8. In reference to Claim 1, Coulson teaches a computer system comprising: a central processing unit (CPU) (See Figure 1 Number 110 and Page 1 Paragraph 17); a first bus coupled to the CPU (See Figure 1 Number 130 and Page 1 Paragraph 17); a memory coupled to the first bus to store data accessible by the CPU via the first bus (See Figure 1 Number 120 and Page 1 Paragraph 17); a second bus coupled to the first bus to provide communication with the CPU and the memory via the first bus (See Figure 1); and a PC card coupled to the second bus (See Page 2 Paragraph 18), the PC card having a non-volatile memory for storing machine state information (See Figure 1 Number 150 and Page 1 Paragraphs 15 and 16) and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figure 1 Number 140 and Pages 1-2 Paragraph 17).

9. In reference to Claim 2, Coulson teaches the limitations as applied to Claim 1 above. Coulson further teaches that the first bus comprises a local CPU bus, as evidenced by its connection to the CPU and the memory (See Figure 1 Number 130); and the second bus comprises a PCI bus, as evidenced by the ability to locate the cache system on a PCI add-in card (See Page 2 Paragraph 18).

10. In reference to Claim 5, Coulson teaches the limitations as applied to Claim 1 above. The device of Coulson would inherently include a bus interface coupled to the second bus and further coupled to the non-volatile memory and the controller to transfer data between the memory and the second bus in accordance with a data format and transfer protocol of the second bus (See Figure 1 and Page 2 Paragraph 18).

11. In reference to Claim 6, Coulson teaches the limitations as applied to Claim 5 above. Coulson further teaches a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information. (See Page 1 Paragraph 16 and Page 2 Paragraph 19).

12. In reference to Claim 8, Coulson teaches the limitations as applied to Claim 1 above. Coulson further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Page 1 Paragraphs 15 and 16).

13. In reference to Claim 9, Coulson teaches a computer system, comprising: a central processing unit (CPU) (See Figure 1 Number 110 and Page 1 Paragraph 17); a memory coupled to the CPU to store data accessible by the CPU (See Figure 1 Number 120 and Page 1 Paragraph 17); a bus coupled to the CPU and memory to provide communication therewith (See Figure 1 Number 130 and Page 1 Paragraph 17); and a

PC card coupled to the bus (See Page 2 Paragraph 18), the PC card having a non-volatile memory for storing machine state information (See Figure 1 Number 150 and Page 1 Paragraphs 15 and 16) and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figure 1 Number 140 and Pages 1-2 Paragraph 17).

14. In reference to Claim 12, Coulson teaches the limitations as applied to Claim 9 above. The device of Coulson would inherently include a bus interface coupled to the second bus and further coupled to the non-volatile memory and the controller to transfer data between the memory and the second bus in accordance with a data format and transfer protocol of the second bus (See Figure 1 and Page 2 Paragraph 18).

15. In reference to Claim 13, Coulson teaches the limitations as applied to Claim 9 above. Coulson further teaches a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information. (See Page 1 Paragraph 16 and Page 2 Paragraph 19).

16. In reference to Claim 15, Coulson teaches the limitations as applied to Claim 9 above. Coulson further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of

operability as when the machine state information was stored in the non-volatile memory (See Page 1 Paragraphs 15 and 16).

17. In reference to Claim 16, Coulson teaches an apparatus for capturing and restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory via a first bus (See Figure 1 Numbers 110, 120, and 130 and Page 1 Paragraph 17), and further having a second bus coupled to the first bus to provide communication with the CPU and the memory (See Figure 1), the apparatus comprising: a PC card coupled to the second bus (See Page 2 Paragraph 18), the PC card having a non-volatile memory for storing machine state information corresponding to the machine state (See Figure 1 Number 150 and Page 1 Paragraphs 15 and 16), and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Figure 1 Number 140 and Pages 1-2 Paragraph 17); and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Page 1 Paragraph 16 and Page 2 Paragraph 19).

18. In reference to Claim 17, Coulson teaches the limitations as applied to Claim 16 above. The device of Coulson would inherently include a bus interface coupled to the second bus and further coupled to the non-volatile memory and the controller to transfer

data between the memory and the second bus in accordance with a data format and transfer protocol of the second bus (See Figure 1 and Page 2 Paragraph 18).

19. In reference to Claim 20, Coulson teaches the limitations as applied to Claim 16 above. Because the device of Coulson loads state information into the non-volatile memory and retrieves said information from the non-volatile memory (See Page 1 Paragraph 16), it inherently includes a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

20. In reference to Claim 22, Coulson teaches an apparatus for capturing and restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory (See Figure 1 Numbers 110, and 120 and Page 1 Paragraph 17), and further having a bus coupled to the CPU and memory to provide communication with the CPU and the memory (See Figure 1 Number 130 and Page 1 Paragraph 17), the apparatus comprising: a PC card coupled to the bus (See Page 2 Paragraph 18), the PC card having a non-volatile memory for storing machine state information corresponding to the machine state (See Figure 1 Number 150 and Page 1 Paragraphs 15 and 16), and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Figure 1 Number 140 and Pages 1-2 Paragraph 17); and a transfer component for directing the controller to

coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Page 1 Paragraph 16 and Page 2 Paragraph 19).

21. In reference to Claim 23, Coulson teaches the limitations as applied to Claim 22 above. The device of Coulson would inherently include a bus interface coupled to the second bus and further coupled to the non-volatile memory and the controller to transfer data between the memory and the second bus in accordance with a data format and transfer protocol of the second bus (See Figure 1 and Page 2 Paragraph 18).

22. In reference to Claim 26, Coulson teaches the limitations as applied to Claim 23 above. Because the device of Coulson loads state information into the non-volatile memory and retrieves said information from the non-volatile memory (See Page 1 Paragraph 16), it inherently includes a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

23. In reference to Claim 38, Coulson teaches a central processing unit (CPU) coupled to a memory (See Figure 1 Numbers 110, and 120 and Page 1 Paragraph 17), and further having a bus coupled to the CPU and memory to provide communication

therewith (See Figure 1 Number 130 and Page 1 Paragraph 17), a method for storing a machine state of the computer system, comprising: capturing the machine state of the computer system (See Page 1 Paragraph 16); transferring machine state information corresponding to the captured machine state from the computer system to a PC card having a non-volatile memory (See Figure 1 Number 150 and Page 2 Paragraphs 18 and 19); and storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system (See Page 1 Paragraph 16).

24. In reference to Claim 42, Coulson teaches the limitations as applied to Claim 38 above. Coulson further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Page 1 Paragraphs 15 and 16).

25. In reference to Claim 45, Coulson teaches a method for restoring a machine state to a computer system having a central processing unit (CPU) coupled to a memory (See Figure 1 Numbers 110, and 120 and Page 1 Paragraph 17), and further having a bus coupled to the CPU and memory to provide communication therewith (See Figure 1 Number 130 and Page 1 Paragraph 17), the method comprising: identifying machine state information corresponding to the machine state to which the computer system is to be restored stored in a non-volatile memory included in a PC card (See

Figure 1 Number 150, Page 1 Paragraph 16, Page 2 Paragraph 18, and Page 3 Paragraph 29); transferring the machine state information from the non-volatile memory to the computer system (See Page 2 Paragraph 19); and writing data of the machine state information to the memory and CPU in order to restore the computer system to the identified machine state (See Page 1 Paragraph 16).

26. In reference to Claim 46, Coulson teaches the limitations as applied to Claim 45 above. Coulson further teaches that identifying, transferring, and writing the machine state information is in response to executing a power up procedure (See Figure 2 and Page 2 Paragraphs 20-22).

27. In reference to Claim 48, Coulson teaches the limitations as applied to Claim 45 above. Coulson further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Page 1 Paragraphs 15 and 16).

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 3, 10, 18, 24, 43, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson as applied to Claims 1, 9, 17, 23, 38, and 48 above, and further in view of US Patent Number 6,256,692 to Yoda et al. ("Yoda").

30. In reference to Claim 3, Coulson teaches the limitations as applied to Claim 2 above. Coulson does not teach a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device coupled to the PCI-CardBus bridge. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 3, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

31. In reference to Claim 10, Coulson teaches the limitations as applied to Claim 9 above. Coulson further teaches that the bus comprises a PCI bus, as evidenced by the ability to locate the cache system on a PCI add-in card (See Page 2 Paragraph 18). Coulson does not teach a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device coupled to the PCI-CardBus bridge. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 10, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

32. In reference to Claim 18, Coulson teaches the limitations as applied to Claim 17 above. Coulson further teaches that the second bus is a PCI bus, as evidenced by the ability to locate the cache system on a PCI add-in card (See Page 2 Paragraph 18). Coulson does not teach that the bus interface is CardBus compatible. Yoda teaches

connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 18, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

33. In reference to Claim 24, Coulson teaches the limitations as applied to Claim 23 above. Coulson further teaches that the second bus is a PCI bus, as evidenced by the ability to locate the cache system on a PCI add-in card (See Page 2 Paragraph 18). Coulson does not teach that the bus interface is CardBus compatible. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 24, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

34. In reference to Claim 43, Coulson teaches the limitations as applied to Claim 38 above. Coulson does not teach that transferring the machine state information to the PC card comprises transferring data from the CPU and the memory to the PC card in accordance with a CardBus protocol. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 43, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices

and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

35. In reference to Claim 49, Coulson teaches the limitations as applied to Claim 48 above. Coulson does not teach that transferring the machine state information from the non-volatile memory comprises transferring data from the PC card to the computer system in accordance with a CardBus protocol. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 49, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

36. Claims 28, 29, 31, 33, 35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson and Yoda.

37. In reference to Claim 28, Coulson teaches a card (See Page 2 Paragraph 18) for restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory via a CPU bus (See Figure 1 Numbers 110, 120, and 130 and Page 1 Paragraph 17), and further having a PCI bus coupled to the CPU bus to provide communication with the CPU and the memory, as evidenced by the ability to locate the cache system on a PCI add-in card (See Page 2 Paragraph 18), the card comprising: a non-volatile memory coupled to the interface for storing and providing machine state information corresponding to the machine state (See Figure 1 Number 150 and Page 1 Paragraphs 15 and 16); a controller coupled to the interface and non-volatile memory to control the storing of machine state information in the non-volatile memory and the retrieval of the machine state information from the non-volatile memory (See Figure 1 Number 140 and Pages 1-2 Paragraph 17); and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Page 1 Paragraph 16 and Page 2 Paragraph 19). The device of Coulson would inherently include an interface coupled to the PCI bus for transferring data thereto and therefrom (See Figure 1 and Page 2 Paragraph 18). Coulson does not teach that the card is a CardBus compatible PC card. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus (See Column 4 Lines 64-66) and connecting the

CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 28, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

38. In reference to Claim 29, Coulson and Yoda teach the limitations as applied to Claim 28 above. Coulson further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Page 1 Paragraphs 15 and 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 29, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices

and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

39. In reference to Claim 31, Coulson and Yoda teach the limitations as applied to Claim 28 above. Because the device of Coulson loads state information into the non-volatile memory and retrieves said information from the non-volatile memory (See Page 1 Paragraph 16), it inherently includes a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 31, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

40. In reference to Claim 33, Coulson teaches a computer system, comprising: a central processing unit (CPU) (See Figure 1 Number 110 and Page 1 Paragraph 17); a local CPU bus coupled to the CPU (See Figure 1 Number 130 and Page 1 Paragraph

17); a memory coupled the local CPU bus to store data accessible by the CPU via the local CPU bus (See Figure 1 Numbers 120 and Page 1 Paragraph 17); a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus, as evidenced by the ability to locate the cache system on a PCI add-in card (See Figure 1 and Page 2 Paragraph 18); a card having a non-volatile memory for storing machine state information corresponding to the machine state (See Figure 1 Number 150 and Page 1 Paragraphs 15 and 16), and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Figure 1 Number 140 and Pages 1-2 Paragraph 17); and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Page 1 Paragraph 16 and Page 2 Paragraph 19). Coulson does not teach a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device and a CardBus compatible PC card coupled to PCI-CardBus bridge. Yoda teaches connecting a non-volatile memory device such as a hard drive to a CardBus card (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the

invention of Claim 33, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

41. In reference to Claim 35, Coulson and Yoda teach the limitations as applied to Claim 33 above. The device of Coulson would inherently include a bus interface coupled to the PCI bus and further coupled to the non-volatile memory and the controller to transfer data between the memory and the PCI bus in accordance with the PCI data format and transfer protocol (See Figure 1 and Page 2 Paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 35, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

42. In reference to Claim 37, Coulson and Yoda teach the limitations as applied to Claim 33 above. Coulson further teaches that the machine state information comprises

data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Page 1 Paragraphs 15 and 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the non-volatile memory of the device of Coulson through the CardBus interface connected to a PCI bus of Yoda, resulting in the invention of Claim 33, because Coulson teaches that the non-volatile memory can be implemented as an add-in card connected to a PCI bus (See Page 2 Paragraph 18 of Coulson), and because the CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

43. Claims 4, 11, 19, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson as applied to Claims 1, 9, 16, and 23 above, and further in view of "The Free On-Line Dictionary of Computing" ("FOLDOC").

44. In reference to Claim 4, Coulson teaches the limitations as applied to Claim 1 above. Coulson does not teach that the non-volatile memory of the PC card comprises a flash memory device. FOLDOC teaches using a flash memory device as a non-volatile storage device (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Coulson using flash memory as the non-

volatile storage, resulting in the invention of Claim 4, because flash memory can be reprogrammed while the chip is installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

45. In reference to Claim 11, Coulson teaches the limitations as applied to Claim 9 above. Coulson does not teach that the non-volatile memory of the PC card comprises a flash memory device. FOLDOC teaches using a flash memory device as a non-volatile storage device (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Coulson using flash memory as the non-volatile storage, resulting in the invention of Claim 11, because flash memory can be reprogrammed while the chip is installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

46. In reference to Claim 19, Coulson teaches the limitations as applied to Claim 16 above. Coulson does not teach that the non-volatile memory comprises a flash memory device. FOLDOC teaches using a flash memory device as a non-volatile storage device (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Coulson using flash memory as the non-volatile storage, resulting in the invention of Claim 19, because flash memory can be

reprogrammed while the chip is installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

47. In reference to Claim 25, Coulson teaches the limitations as applied to Claim 23 above. Coulson does not teach that the non-volatile memory comprises a flash memory device. FOLDOC teaches using a flash memory device as a non-volatile storage device (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Coulson using flash memory as the non-volatile storage, resulting in the invention of Claim 25, because flash memory can be reprogrammed while the chip is installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

48. Claims 7, 14, 21, 27, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson as applied to Claims 1, 9, 16, 23, and 38 above, and further in view of US Patent Number 5,875,454 to Craft et al. ("Craft").

49. In reference to Claim 7, Coulson teaches the limitations as applied to Claim 1 above. Coulson does not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Craft teaches a cache memory in which data is compressed prior to storage in the cache and

decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the compression and decompression system for cache storage of Craft, resulting in the invention of Claim 7, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

50. In reference to Claim 14, Coulson teaches the limitations as applied to Claim 9 above. Coulson does not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Craft teaches a cache memory in which data is compressed prior to storage in the cache and decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the compression and decompression system for cache storage of Craft, resulting in the invention of Claim 14, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

51. In reference to Claim 21, Coulson teaches the limitations as applied to Claim 16 above. Coulson does not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Craft teaches a cache memory in which data is compressed prior to storage in the cache and decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the compression and decompression system for cache storage of Craft, resulting in the invention of Claim 21, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

52. In reference to Claim 27, Coulson teaches the limitations as applied to Claim 23 above. Coulson does not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Craft teaches a cache memory in which data is compressed prior to storage in the cache and decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the compression and

decompression system for cache storage of Craft, resulting in the invention of Claim 27, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

53. In reference to Claim 44, Coulson teaches the limitations as applied to Claim 38 above. Coulson does not teach compressing the machine state information to be stored in the non-volatile memory. Craft teaches a cache memory in which data is compressed prior to storage in the cache (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the compression system for cache storage of Craft, resulting in the invention of Claim 44, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

54. Claims 30 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson and Yoda as applied to Claims 28 and 33 above, and further in view of FOLDOC.

55. In reference to Claim 30, Coulson and Yoda teach the limitations as applied to Claim 28 above. Coulson and Yoda do not teach that the non-volatile memory comprises a flash memory device. FOLDOC teaches using a flash memory device as a

non-volatile storage device (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Coulson and Yoda using flash memory as the non-volatile storage, resulting in the invention of Claim 30, because flash memory can be reprogrammed while the chip is installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

56. In reference to Claim 34, Coulson and Yoda teach the limitations as applied to Claim 33 above. Coulson and Yoda do not teach that the non-volatile memory of the PC card comprises a flash memory device. FOLDOC teaches using a flash memory device as a non-volatile storage device (See entry 'Flash Erasable Programmable Read-Only Memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Coulson and Yoda using flash memory as the non-volatile storage, resulting in the invention of Claim 34, because flash memory can be reprogrammed while the chip is installed (See entry 'Flash Erasable Programmable Read-Only Memory' in FOLDOC).

57. Claims 32, 36, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson and Yoda as applied to Claims 28, 33, and 45 above, and further in view of Craft.

58. In reference to Claim 32, Coulson and Yoda teach the limitations as applied to Claim 28 above. Coulson and Yoda do not teach compression and decompression components for compressing the machine state information to be stored in the non-volatile memory and decompressing the stored compressed machine state information to be downloaded, respectively. Craft teaches a cache memory in which data is compressed prior to storage in the cache and decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson and Yoda with the compression and decompression system for cache storage of Craft, resulting in the invention of Claim 32, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

59. In reference to Claim 36, Coulson and Yoda teach the limitations as applied to Claim 33 above. Coulson and Yoda do not teach compression and decompression components for compressing the machine state information to be stored in the non-volatile memory and decompressing the stored compressed machine state information to be downloaded, respectively. Craft teaches a cache memory in which data is compressed prior to storage in the cache and decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson and Yoda with the compression and decompression system for cache storage of Craft, resulting in the invention of Claim 36, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

60. In reference to Claim 50, Coulson and Yoda teach the limitations as applied to Claim 45 above. Coulson and Yoda do not teach that the machine state information stored in the non-volatile memory is in a compressed data format, and decompressing the machine state information to be transferred to the computer system. Craft teaches a cache memory in which data is compressed prior to storage in the cache and decompressed upon retrieval from the cache before being sent to the computer system (See Column 3 Lines 31-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson and Yoda with the compression and decompression system for cache storage of Craft, resulting in the invention of Claim 50, because compressing data for storage in a cache is a recognized desirable design objective (See Column 2 Lines 1-9 of Craft).

61. Claims 39 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson as applied to Claims 38 and 45 above, and further in view of US Patent Number 6,186,400 to Dvorkis et al. ("Dvorkis").

62. In reference to Claim 39, Coulson teaches the limitations as applied to Claim 38 above. Coulson does not teach that capturing, transferring, and storing the machine state information is in response to executing a power down procedure. Coulson does teach that the process does not need to be performed during system initialization (See Page 3 Paragraph 29). Dvorkis teaches saving the status of a system in response to executing a power down procedure (See Column 11 Lines 52-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the status save at power down of Dvorkis, resulting in the invention of Claim 39, in order to protect the system from sudden shocks by allowing it to save its state and shut down when a shock is detected (See Column 11 Line 52 – Column 12 Line 10 of Dvorkis).

63. In reference to Claim 47, Coulson teaches the limitations as applied to Claim 45 above. Coulson does not teach that identifying, transferring, and writing the machine state information is in response to a user request. Dvorkis teaches restoring the system state based on a user request (See Column 12 Lines 1-10)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the user requested state restore of Dvorkis, resulting in the invention of Claim 47, in order to allow the user to determine whether to resume the system from the point when the shutdown occurred or to continue from a different point (See Column 12 Lines 1-12 of Dvorkis).

64. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson as applied to Claim 38 above, and further in view of US Patent Number 6,438,668 to Esfahani et al. ("Esfahani").

65. In reference to Claim 40, Coulson teaches the limitations as applied to Claim 38 above. Coulson does not teach that capturing, transferring, and storing the machine state information is in response to a user request. Esfahani teaches a user instruction to the system to save the state to a non-volatile memory device (See Column 1 Lines 50-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the user requested state save of Esfahani, resulting in the invention of Claim 40, in order to allow the user to return the system to a certain operating condition when the off state was entered (See Column 1 Lines 55-59 of Esfahani).

66. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coulson as applied to Claim 38 above, and further in view of US Patent Number 6,243,831 to Mustafa et al. ("Mustafa").

67. In reference to Claim 42, Coulson teaches the limitations as applied to Claim 38 above. Coulson does not teach that capturing the machine state of the computer

system comprises capturing data present in the memory and capturing data present in the registers of the CPU. Mustafa teaches saving the contents of registers and memory upon entering a power saving mode (See Column 2 Lines 55-64 and Column 3 Lines 22-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Coulson with the register and memory save of Mustafa, resulting in the invention of Claim 42, in order to allow the state of the computer prior to disruption of power to be restored (see Column 3 Lines 1-4 of Mustafa).

Drawings

68. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 4 Number 426. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

69. The information disclosure statement filed 28 August 2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

70. Applicant's assistance is requested in identifying any prior art which is believed to be of particular relevance to the present application.

Conclusion

71. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 6,233,376 to Updegrove.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thomas J. Cleary
Patent Examiner
Art Unit 2111